vided within the linear active cell area and divided in a longitudinal direction thereof.

2. The IE-type trench gate IGBT according to claim **1** wherein the width of the linear active cell area is narrower than the width of the linear inactive cell area.

3. The IE-type trench gate IGBT according to claim **2**,

wherein a second conductivity type floating region of a conductivity type opposite to the first conductivity type is provided in a surface region on the first main surface side, of the drift region in the linear inactive cell area approximately over a whole area thereof, and

wherein the second conductivity type floating region covers lower ends of the pair of trenches and is deeper than the pair of trenches in depth.

4. The IE-type trench gate IGBT according to claim **3**, wherein each of the linear unit cell areas comprises a plurality of blocks which form longitudinal direction columns thereof, the each block comprising:

(x1) an active subblock comprising the active section;

(x2) an inactive subblock free of the active section;

(x3) a coupling trench gate electrode which couples between the pair of linear trench gate electrodes and separates the active subblock and the inactive subblock from each other; and

(x4) an emitter contact portion unprovided in the inactive subblock and provided in the active subblock.

5. The IE-type trench gate IGBT according to claim **4**, wherein the active section is provided at part of the active subblock.

6. The IE-type trench gate IGBT according to claim **4**, wherein the active sections are provided over a full range of the active subblock.

7. The IE-type trench gate IGBT according to claim **3**, wherein the linear inactive cell area comprises:

(y1) a first conductivity type floating region formation section which is divided in a longitudinal direction of the linear inactive cell area and which is formed in the surface region thereof on the first main surface side and provided with a first conductivity type floating region of the same conductivity type as the first conductivity type; and

(y2) a first conductivity type floating region non-formation section which is divided in a longitudinal direction of the linear inactive cell area and which is formed in the surface region thereof on the first main surface side and unprovided with the first conductivity type floating region.

8. The IE-type trench gate IGBT according to claim **3**, wherein a first conductivity type floating region of the same conductivity type as the first conductivity type is provided in the surface region on the first main surface side, of the linear inactive cell area approximately over a whole area thereof.

9. The IE-type trench gate IGBT according to claim **5**, wherein a first conductivity type floating region of the same conductivity type as the first conductivity type is provided in the surface region on the first main surface side, of each of the inactive subblock and the linear inactive cell area approximately over a whole area thereof.

10. An IE-type trench gate IGBT comprising:

(a) a semiconductor substrate comprising a first main surface and a second main surface;

(b) a drift region of a first conductivity type provided within the semiconductor substrate;

(c) a cell area provided over the first main surface; and

(d) a number of linear unit cell areas provided within the cell area as seen on a plane basis;

wherein the each linear unit cell area comprises:

(d1) a linear active cell area provided from over the first main surface in the drift region to the inside thereof;

(d2) a pair of linear trench gate electrodes lying within a pair of trenches provided in the surface of the first main surface so as to sandwich the linear active cell area therebetween from both sides as seen on a plane basis;

(d3) a second conductivity type body region of a conductivity type opposite to the first conductivity type, the second conductivity type body region being provided in a surface region on the first main surface side, of the drift region;

(d4) linear inactive cell areas provided adjacent to each other on both sides so as to sandwich the linear active cell area therebetween from both sides thereof on a plane basis with the pair of linear trench gate electrodes as boundaries;

(d5) a first conductivity type emitter region of the same conductivity type as the first conductivity type, the first conductivity type emitter region being provided in a surface region on the first main surface side, of the second conductivity type body region in the linear active cell area;

(d6) a first conductivity type hole barrier region being of the same conductivity type as the first conductivity type, provided in the drift region lying underneath the second conductivity type body region in the linear active cell area, the first conductivity type hole barrier region being higher than the drift region and lower than the first conductivity type emitter region in impurity concentration; and

(d7) a second conductivity type floating region of a conductivity type opposite to the first conductivity type, the second conductivity type floating region being provided approximately over a whole area of the surface region on the first main surface side in the linear inactive cell area,

wherein the second conductivity type floating region covers lower ends of the pair of trenches and is deeper than the pair of trenches in depth.

11. The IE-type trench gate IGBT according to claim **10**, wherein the width of each of the pair of trenches is less than or equal to 0.8 micrometers.

12. The IE-type trench gate IGBT according to claim **10**, wherein the second conductivity type floating region is formed simultaneously with a floating field ring at an outer periphery of the cell area.

13. The IE-type trench gate IGBT according to claim **10**, wherein the thicknesses of gate insulating films on both sides of each of the pair of linear trench gate electrodes are substantially the same.

14. An IE-type trench gate IGBT comprising:

(a) a semiconductor substrate comprising a first main surface and a second main surface;

(b) a drift region of a first conductivity type provided within the semiconductor substrate;

(c) a cell area provided over the first main surface;

(d) a number of linear unit cell areas provided within the cell area as seen on a plane basis;

(e) a metal collector electrode provided over the second main surface of the semiconductor substrate;

(f) a second conductivity type collector region of a conductivity type opposite to the first conductivity type, the